Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-80 (Cancelled).

81. (Currently Amended) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND ~~logic~~ gate having ~~an internal circuit node,~~ a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND ~~logic~~ gate having ~~an internal circuit node,~~ a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs ~~between the internal node of the first logic gate and the internal node of the second logic gate~~, and

wherein the ferroelectric capacitor circuit comprises a first ferroelectric capacitor coupled between the Q output and ground, a second ferroelectric capacitor coupled between the complementary Q output and ground; and a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

82. (New) The SR flip-flop of claim 81 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

83. (New) The SR flip-flop of claim 81 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

84. (New) The SR flip-flop of claim 81 further comprising a precharge circuit coupled to the first and second NAND gates.

85. (New) The SR flip-flop of claim 81 further comprising an equalization circuit coupled to the first and second NAND gates.

86. (New) The SR flip-flop of claim 81 further comprising a gate control circuit coupled to the first and second NAND gates.

87. (New) The SR flip-flop of claim 81 in which the first and second NAND gates further comprise an internal drive isolation circuit.

88. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs, and

wherein the ferroelectric capacitor circuit comprises a first ferroelectric capacitor coupled between the Q output and ground, a second ferroelectric capacitor coupled between the complementary Q output and ground, and third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

89. (New) The SR flip-flop of claim 88 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

90. (New) The SR flip-flop of claim 88 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

91. (New) The SR flip-flop of claim 88 further comprising a precharge circuit coupled to the first and second NAND gates.

92. (New) The SR flip-flop of claim 88 further comprising an equalization circuit coupled to the first and second NAND gates.

93. (New) The SR flip-flop of claim 88 further comprising a gate control circuit coupled to the first and second NAND gates.

94. (New) The SR flip-flop of claim 88 in which the first and second NAND gates further comprise an internal drive isolation circuit.

95. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs; and

means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

96. (New) The SR flip-flop of claim 95 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

97. (New) The SR flip-flop of claim 95 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

98. (New) The SR flip-flop of claim 95 further comprising a precharge circuit coupled to the first and second NAND gates.

99. (New) The SR flip-flop of claim 95 further comprising an equalization circuit coupled to the first and second NAND gates.

100. (New) The SR flip-flop of claim 95 further comprising a gate control circuit coupled to the first and second NAND gates.

101. (New) The SR flip-flop of claim 95 in which the first and second NAND gates further comprise an internal drive isolation circuit.

102. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs; and

a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

103. (New) The SR flip-flop of claim 102 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

104. (New) The SR flip-flop of claim 102 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

105. (New) The SR flip-flop of claim 102 further comprising a precharge circuit coupled to the first and second NAND gates.

106. (New) The SR flip-flop of claim 102 further comprising an equalization circuit coupled to the first and second NAND gates.

107. (New) The SR flip-flop of claim 102 further comprising a gate control circuit coupled to the first and second NAND gates.

108. (New) The SR flip-flop of claim 102 in which the first and second NAND gates further comprise an internal drive isolation circuit.

109. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NAND gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NAND gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs, and

wherein the first and second NAND gates further comprise an internal drive isolation circuit.

110. (New) The SR flip-flop of claim 109 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

111. (New) The SR flip-flop of claim 109 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

112. (New) The SR flip-flop of claim 109 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

113. (New) The SR flip-flop of claim 109 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and

complementary Q outputs.

114. (New) The SR flip-flop of claim 109 further comprising a precharge circuit coupled to the first and second NAND gates.

115. (New) The SR flip-flop of claim 109 further comprising an equalization circuit coupled to the first and second NAND gates.

116. (New) The SR flip-flop of claim 109 further comprising a gate control circuit coupled to the first and second NAND gates.

117. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs, and

wherein the ferroelectric capacitor circuit comprises a first ferroelectric capacitor coupled between the Q output and ground, a second ferroelectric capacitor coupled between the complementary Q output and ground; and a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

118. (New) The SR flip-flop of claim 117 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

119. (New) The SR flip-flop of claim 117 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

120. (New) The SR flip-flop of claim 117 further comprising a precharge circuit coupled to the first and second NOR gates.

121. (New) The SR flip-flop of claim 117 further comprising an equalization circuit coupled to the first and second NOR gates.

122. (New) The SR flip-flop of claim 117 further comprising a gate control circuit coupled to the first and second NOR gates.

123. (New) The SR flip-flop of claim 117 in which the first and second NOR gates further comprise an internal drive isolation circuit.

124. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs, and

wherein the ferroelectric capacitor circuit comprises a first ferroelectric capacitor coupled between the Q output and ground, a second ferroelectric capacitor coupled between the complementary Q output and ground, and third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

125. (New) The SR flip-flop of claim 124 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

126. (New) The SR flip-flop of claim 124 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

127. (New) The SR flip-flop of claim 124 further comprising a precharge circuit coupled to the first and second NOR gates.

128. (New) The SR flip-flop of claim 124 further comprising an equalization circuit coupled to the first and second NOR gates.

129. (New) The SR flip-flop of claim 124 further comprising a gate control circuit coupled to the first and second NOR gates.

130. (New) The SR flip-flop of claim 124 in which the first and second NAND gates further comprise an internal drive isolation circuit.

131. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs; and

means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

132. (New) The SR flip-flop of claim 131 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

133. (New) The SR flip-flop of claim 131 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

134. (New) The SR flip-flop of claim 131 further comprising a precharge circuit coupled to the first and second NOR gates.

135. (New) The SR flip-flop of claim 131 further comprising an equalization circuit coupled to the first and second NOR gates.

136. (New) The SR flip-flop of claim 131 further comprising a gate control circuit coupled to the first and second NOR gates.

137. (New) The SR flip-flop of claim 131 in which the first and second NOR gates further comprise an internal drive isolation circuit.

138. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs; and

a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

139. (New) The SR flip-flop of claim 138 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

140. (New) The SR flip-flop of claim 138 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

141. (New) The SR flip-flop of claim 138 further comprising a precharge circuit coupled to the first and second NOR gates.

142. (New) The SR flip-flop of claim 138 further comprising an equalization circuit coupled to the first and second NOR gates.

143. (New) The SR flip-flop of claim 138 further comprising a gate control circuit coupled to the first and second NOR gates.

144. (New) The SR flip-flop of claim 138 in which the first and second NOR gates further comprise an internal drive isolation circuit.

145. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first NOR gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second NOR gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output; and

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs, and

wherein the first and second NOR gates further comprise an internal drive isolation circuit.

146. (New) The SR flip-flop of claim 145 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

a third ferroelectric capacitor coupled between the Q and complementary Q outputs.

147. (New) The SR flip-flop of claim 145 in which the ferroelectric capacitor circuit comprises:

a first ferroelectric capacitor coupled between the Q output and ground;

a second ferroelectric capacitor coupled between the complementary Q output and ground; and

third and fourth serially-coupled matched ferroelectric capacitors coupled between the Q and complementary Q outputs.

148. (New) The SR flip-flop of claim 145 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

149. (New) The SR flip-flop of claim 145 further comprising a pass gate circuit for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

150. (New) The SR flip-flop of claim 145 further comprising a precharge circuit coupled to the first and second NOR gates.

151. (New) The SR flip-flop of claim 145 further comprising an equalization circuit coupled to the first and second NOR gates.

152. (New) The SR flip-flop of claim 145 further comprising a gate control circuit coupled to the first and second NOR gates.

153. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first logic gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second logic gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit comprising first, second, and third ferroelectric capacitors, including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs;

a J input;

a K input;

a first NAND gate having a first input coupled to the Q output of the SR flip-flop, a second input coupled to the K input, a third input for receiving a clock signal and an output coupled to the set input of the SR flip-flop; and

a second NAND gate having a first input for receiving the clock signal, a second input coupled to the J input, a third input coupled to the complementary Q output of the SR flip-flop and an output coupled to the reset input of the SR flip-flop.

154. (New) The SR flip-flop of claim 153 further comprising a first controlled power supply coupled to the SR flip-flop.

155. (New) The SR flip-flop of claim 154 further comprising a second controlled power supply coupled to the SR flip-flop.

156. (New) The SR flip-flop of claim 153 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

157. (New) The SR flip-flop of claim 153 further comprising a precharge circuit coupled to the SR flip-flop.

158. (New) The SR flip-flop of claim 153 further comprising an equalization circuit coupled to the SR flip-flop.

159. (New) The SR flip-flop of claim 153 further comprising a gate control circuit coupled to the SR flip-flop.

160. (New) The SR flip-flop of claim 153 in which the SR flip-flop further comprises an internal drive isolation circuit.

161. (New) The SR flip-flop of claim 153 further comprising:

a slave JK flip-flop interposed between the Q output and the complementary Q output, and the first input of the first NAND gate and the third input of the second NAND gate.

162. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first logic gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second logic gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs;

a J input;

a K input;

a first NAND gate having a first input coupled to the Q output of the SR flip-flop, a second input coupled to the K input, a third input for receiving a clock signal and an output coupled to the set input of the SR flip-flop; and

a second NAND gate having a first input for receiving the clock signal, a second input coupled to the J input, a third input coupled to the complementary Q output of the SR flip-flop and an output coupled to the reset input of the SR flip-flop,

wherein the SR flip-flop further comprises an internal drive isolation circuit.

163. (New) The SR flip-flop of claim 162 further comprising a first controlled power supply coupled to the SR flip-flop.

164. (New) The SR flip-flop of claim 163 further comprising a second controlled power supply coupled to the SR flip-flop.

165. (New) The SR flip-flop of claim 162 in which the ferroelectric capacitor circuit comprises first, second, and third ferroelectric capacitors.

166. (New) The SR flip-flop of claim 162 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

167. (New) The SR flip-flop of claim 162 further comprising a precharge circuit coupled to the SR flip-flop.

168. (New) The SR flip-flop of claim 162 further comprising an equalization circuit coupled to the SR flip-flop.

169. (New) The SR flip-flop of claim 162 further comprising a gate control circuit coupled to the SR flip-flop.

170. (New) The SR flip-flop of claim 162 further comprising:

a slave JK flip-flop interposed between the Q output and the complementary Q output, and the first input of the first NAND gate and the third input of the second NAND gate.

171. (New) A ferroelectric, non-volatile, SR flip-flop comprising:

a set input;

a reset input;

a Q output;

a complementary Q output;

a first logic gate having a first input coupled to the set input, a second input coupled to the output, and an output coupled to the complementary Q output;

a second logic gate having a first input coupled to the reset input, a second input coupled to the complementary Q output, and an output coupled to the Q output;

a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled to the Q and complementary Q outputs;

a J input;

a K input;

a first NAND gate having a first input coupled to the Q output of the SR flip-flop, a second input coupled to the K input, a third input for receiving a clock signal and an output coupled to the set input of the SR flip-flop;

a second NAND gate having a first input for receiving the clock signal, a second input coupled to the J input, a third input coupled to the complementary Q output of the SR flip-flop and an output coupled to the reset input of the SR flip-flop; and

a slave JK flip-flop interposed between the Q output and the complementary Q output, and the first input of the first NAND gate and the third input of the second NAND gate.

172. (New) The SR flip-flop of claim 171 further comprising a first controlled power supply coupled to the SR flip-flop.

173. (New) The SR flip-flop of claim 172 further comprising a second controlled power supply coupled to the SR flip-flop.

174. (New) The SR flip-flop of claim 171 in which the ferroelectric capacitor circuit comprises first, second, and third ferroelectric capacitors.

175. (New) The SR flip-flop of claim 171 further comprising means for selectively coupling the ferroelectric capacitor circuit to the Q and complementary Q outputs.

176. (New) The SR flip-flop of claim 171 further comprising a precharge circuit coupled to the SR flip-flop.

177. (New) The SR flip-flop of claim 171 further comprising an equalization circuit coupled to the SR flip-flop.

178. (New) The SR flip-flop of claim 171 further comprising a gate control circuit coupled to the SR flip-flop.

179. (New) The SR flip-flop of claim 171 in which the SR flip-flop further comprises an internal drive isolation circuit.